REMARKS/ARGUMENTS

Claims 1-22 remain pending in this application and stand rejected. Claims 1, 3-4, 7-8, 12, 14-15 and 19 stand rejected under 35 U.S.C. 102(b) as being anticipated by Mahoney et al. (USPN 5,694,056); hereinafter Mahoney. Claim 5-8, 9-11, 16-17 and 20-22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mahoney. Claims 1 and 13 are objected to as being dependent upon a rejected base claim but are indicated as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In view of the foregoing amendments and following remarks, reconsideration of the rejections of claims 1-22 is respectfully requested.

Claim 1 is amended to recite, in part, "transferring a start read address ... via data lines...". Support for this limitation is provided, for example, on page 4, lines 17-20; page 5, lines 1-2; page 5, lines 10-12; page 2, lines 13-14; etc., and reproduced below for the Examiner's convenience:

"FPGA 120 transfers an 8-bit start read address to FLASH memory device 121 along signal lines DQ[7:0] after the Sequential-Mode-Command as shown in Figure 2B. Signal lines DQ can include any suitable number of signal lines, for example 16, if 16-bit parallel data transfer is desired.." (4:17-20)

"In another embodiment, Sequential Read Mode can be entered by sending an instruction code via data lines DQ..." (5:1-2)

"In response to each new read address, FLASH memory 121 accesses a byte of data from its memory array and transfers that data byte along parallel signal lines DQ to FPGA 120" (5:10-12)

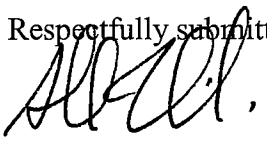
"Instead, the destination circuit interfaces directly with the memory device using less pins than prior art techniques" (2:13-14)

Support for the amendment to claim 1 is also provided in Figure 1. As is seen from Figure 1, flash memory 121 receives clock signal CLK and command signals CEO and OE# from FPGA 120. Flash memory 121 also communicates with FPGA 102 via data lines DQ which FPGA 120 also uses to supply "a start read address" to flash memory 121, as recited in claim1. In other words, in accordance with the present invention, the data lines DQ are also used to supply the starting address and hence no separate address lines are needed, thus eliminating the need for extra address pins.

Mahoney, on the other hand, is directed at increasing the data rate transfer and not at minimizing the number of pins. There is no disclosure in the Abstract, column 1, lines 65 et seq., column 2, lines 7-19, of Mahoney of transferring a start read address from the integrated circuit "via data lines" to the external memory device. Claim 1 and its dependent claims 2-11 are thus allowable for at least the reasons cited above. Claim 12 is also amended to recite, in part, "...generates read addresses beginning with the start read address supplied from the integrated circuit via data line.." Consequently, claim 12 and its dependent claims 13-22 are allowable for at least the same reasons as is claim 1.

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (650) 752-2424.

Respectfully submitted,



Ardeshir Tabibi
Reg. No. 48,750

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (650) 326-2400
Fax: (650) 326-2422
AT:deh
60966000 v1